What is claimed is:

[Claim 1] A gated semiconductor device, comprising:

a fin-shaped body having a first dimension extending in a lateral direction parallel to a major surface of a substrate, and second dimension extending in a direction at least substantially vertical and at least substantially perpendicular to the major surface, the body having a first side and a second side opposite the first side;
a first gate overlying the first side, the first gate having a first gate length in the lateral direction; and
a second gate overlying the second side, the second gate having a second gate length in the lateral direction which is different from the first gate length, the second gate being electrically isolated from the first gate.

[Claim 2] The gated semiconductor device as claimed in claim 1, wherein the first gate consists essentially of polycrystalline silicon germanium and the second gate consists essentially of polysilicon.

[Claim 3] A gated semiconductor device, comprising:

a fin-shaped body having a first dimension extending in a lateral direction parallel to a major surface of a substrate, and second dimension extending in a direction at least substantially vertical and at least substantially perpendicular to the major surface, the body having a first side and a second side opposite the first side;
a first gate consisting essentially of polycrystalline silicon germanium overlying the first side, the first gate having a first gate length in the lateral direction; and
a second gate consisting essentially of polysilicon overlying the second side, the second gate having a second gate length in the lateral direction which is

different from the first gate length, the second gate being electrically isolated from the first gate.

[Claim 4] The gated semiconductor device as claimed in claim 3, wherein the first gate length is substantially shorter than the second gate length such that the first gate has lower gate capacitance relative to the body than the second gate.

[Claim 5] The gated semiconductor device as claimed in claim 3, further comprising a first gate dielectric disposed on the first side underlying the first gate, and a second gate dielectric disposed on the second side underlying the second gate.

[Claim 6] The gated semiconductor device as claimed in claim 3, further comprising a first oxide region including at least one of an oxide of silicon and an oxide of germanium disposed laterally adjacent to the first gate.

[Claim 7] The gated semiconductor device as claimed in claim 6, further comprising a second oxide region including an oxide of silicon disposed laterally adjacent to the second gate.

[Claim 8] The gated semiconductor device as claimed in claim 7, further comprising a first spacer disposed laterally adjacent to the first oxide region and a second spacer disposed laterally adjacent to the second oxide region.

[Claim 9] The gated semiconductor device as claimed in claim 8, wherein the body is disposed in a semiconductor-on-insulator (SOI) layer of an SOI substrate.

[Claim 10] The gated semiconductor device as claimed in claim 9, wherein the first gate and the second gate contact a buried oxide (BOX) layer of the substrate underlying the SOI layer.

[Claim 11] The gated semiconductor device as claimed in claim 10, wherein the body is electrically insulated from the first gate and the second gate by the BOX layer, the first gate dielectric, the second gate dielectric and a dielectric cap disposed over a top side of the body.

[Claim 12] The gated semiconductor device as claimed in claim 4, further comprising a source disposed at one end of the body, and a drain disposed at another end of the body opposite the one end, wherein the body has predominantly a first dopant type selected from n-type and p-type and the source and drain both have predominantly a second dopant type selected from n-type and p-type, the second dopant type being different from the first dopant type.

[Claim 13] The gated semiconductor device as claimed in claim 12, wherein the second gate is conductively connected to one of the source and the drain such that the gated semiconductor device is operable as a gated diode.

[Claim 14] The gated semiconductor device as claimed in claim 12, wherein the gated semiconductor device is operable as an insulated gate field effect transistor (FET), wherein the first gate is operable to apply a bias to adjust a threshold voltage of the FET.

[Claim 15] The gated semiconductor device as claimed in claim 3, further comprising a first gate polysilicon layer overlying the first gate.

[Claim 16] The gated semiconductor device as claimed in claim 15, further comprising a first silicide region disposed on the first gate polysilicon layer and a second silicide region disposed on the second gate.

[Claim 17] The gated semiconductor device as claimed in claim 16, further comprising a first conductive via contacting the first silicide region and a second conductive via conductive via contacting the second silicide region.

[Claim 18] An integrated circuit including the gated semiconductor device as claimed in claim 1.

[Claim 19] A method of making a gated semiconductor device, comprising:

patterning a single-crystal semiconductor region of a substrate to extend in a lateral direction parallel to a major surface of a substrate and to extend in a direction at least substantially vertical and at least substantially perpendicular to the major surface, the semiconductor region having a first side and a second side opposite the first side;
forming a first gate overlying the first side, the first gate having a first gate length in the lateral direction; and
forming a second gate overlying the second side, the second gate having a second gate length in the lateral direction which is different from the first gate length, the second gate being electrically isolated from the first gate.

[Claim 20] The method as claimed in claim 19, wherein the first gate is formed to consist essentially of polycrystalline silicon germanium and the second gate is formed to consist essentially of polysilicon.

[Claim 21] The method as claimed in claim 20, wherein the first gate and the second gate are formed by:

forming a first region consisting essentially of polycrystalline silicon germanium overlying the first side;
thereafter forming a second region consisting essentially of polysilicon overlying the second side and insulated from the first region;
simultaneously lithographically patterning the first region and the second region using a given opening of a given lithographic mask, and
thereafter simultaneously thermally oxidizing the first region to form the first gate and the second region to form the second gate.

[Claim 22] The method as claimed in claim 21, wherein the first region is thermally oxidized at a faster rate than the second region, causing the first gate length to be shorter than the second gate length.